REMARKS

Reconsideration of the above referenced application in view of the following remarks is requested. Claims 2 and 32 were previously cancelled. Existing claims 1, 3-31, and 33 (as amended) remain in the application.

ARGUMENT

Claim Rejections – 35 USC § 103

Claims 1, 3-10, and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (6,629,268) (hereinafter Arimilli_1) in view of WO 00/52582 (hereinafter WO reference) and further in view of Arimilli (2002/0129211) (hereinafter Arimilli_2).

In the Examiner's response to Applicant's arguments regarding the limitation of "two cache coherency states associated with one cache line" filed on April 23, 2007, the Examiner asserted Fig. 1, p.6 et seq., page 7, par. 4, Fig. 3, and page 12 of the WO reference as disclosing this limitation. Applicants respectfully disagree.

The Examiner stated, "Fig. 1 of WO clearly shows a cache (CS) assessable by a plurality of processors (EPs) through a first interface (BS1) on one side and accessible by additional cache memories, main memory (MEM), or all types of I/O through a second interface (BS2). If a line was recently cached from main memory (MEM) through BS2, said cache line is in the exclusive state, and if one of the processors (EPs) wants to read the cache line, and performs some operation that require **changing the state of the cache to modified**, another associated processor (EP) trying to read the

same cache line through interface BS1 would find it in a modified state" (emphasis added). The Examiner is right that the CS shown in Fig. 1 of the WO reference is accessible from either BS1 or BS2. However, Applicants' arguments were not about this point. Applicants argued that the cache line has two cache coherency states. This feature is not disclosed by the WO reference at all. In the Examiner's statements quoted above, it is very clear that a cache line has only one coherency state at one time. The example quoted by the Examiner clearly states that an "E" state will be required to change to an "M" state. In other words, the cache line cannot have both the "E" state and the "M" state at the same time. Thus, Fig. 1, p. 6 et seq. of the WO reference does not teach or suggest this limitation.

Second, the Examiner cited page 7, par. 4 of the WO reference as disclosing the limitation of "a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface." Applicants respectfully disagree. There are gaps between the Examiner's arguments here. For example, the Examiner quoted from the WO reference, "requests can be made between the additional cache memories CS and the individual processors EP," based on this statement the Examiner concluded that "through interface BS1 processors EP guarantee access of a cache line with a first coherency state." Of course that EPs in Fig. 1 can access CS. The key is that the statement above quoted by the Examiner from the WO reference and the rest of the WO reference do not teach or suggest that EP access a cache line in the CS using one of the two coherency states of the cache line because a cache line in the CS has only one coherency state at one time. And there are no two cache coherency states associated with a cache line at the same time

in the WO reference. Similarly, the Examiner jumped to a conclusion—"through cache memory bus BS2 guarantee accessing a cache line with a second coherency state" from a statement from the WO reference—"requests between additional cache memories CS and the main memory." Please note that although the WO does disclose that the CS can be accessed from BS2, it does not teach or suggest that such an access to a cache line in the CS through BS2 is through one of the two cache coherency states of the cache line. Again the cache line does not have two coherency states associated with it at the same time. It is impossible for an access to a cache line in the CS through BS1 and through BS2 using two different cache coherency states. Thus, page 7, par. 4 of the WO reference does not teach or suggest the limitation of "a first cache coherency state when accessed from said first interface and a second cache coherency state when accessed from said second interface."

Third, the Examiner asserted, "the WO reference discloses unequivocally in Fig. 3 a state diagram having the expanded states SI, ES, MI, MS, II, SS, EM, and MM, the first letter of a state title relating to the state in the TLC, while the second letter relates to the state in the SLC and/or in a lower cache hierarchy state." Fig. 3 of the WO reference does have expanded states. However, the WO reference, as quoted by the Examiner makes it very clear: "the first letter of a state title relates to the state in the TLC, while the second letter relates to the state in the SLC and/or in a lower cache hierarchy stage." In other words, the expanded states are not two coherency states for a cache line in the same cache. It is simply a combination of a coherency state of a cache line in the CS and a coherency state of the corresponding cache line in SLC. As defined by the WO reference, SLC is identified as the cache hierarchy which is formed

by the two cache memories of an individual processor while TLC is identified as the additional cache memories (CS) (see page 7, paragraphs 1 and 2 of the WO reference). Paragraph 3 on page 12 of the WO reference provides an example explaining why there is no EE entry. From this example, it is clear that an "EM" expanded state refers to "E" state of a cache line in SLC and "M" state of the superset of the cache line in the TSL (SC). Additionally, the Examiner is invited to review the table in Figure 3 of the WO reference which shows what an expanded state means. For example, an ES state means that a cache line in TLC has "E" state and its corresponding cache line in the SLC has either an "I" state or an "S" state. Expanded states are simply used to optimize state transition diagram (see page 12 and 13 of the WO reference). Thus, the expanded states shown in Fig. 3 and its corresponding description in the specification do not mean that a cache line in any single cache has two coherency states, as recited in the independent claims in the present application, but only means the state of the cache line in a processor's cache (SLC) and the state of the cache line's superset in additional cache (TLC) (outer-layer cache compared to the processor's cache).

For the forgoing, the WO reference does not teach or suggest all of the limitations recited in independent claim 1 or 31. Arimilli_1 or Arimilli_2 was not cited to cure those deficiencies of the WO reference. Thus, claims 1 and 31 are patentable of the combination of the cited references. Accordingly, all of the claims that depend therefrom (i.e., claims 3-10, and claim 33, respectfully) are also patentable over the combination of the cited references.

Claims 11-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli_2 in view of the WO reference.

In the Examiner's response to Applicants' arguments filed on April 23, 2007, the Examiner stated, "The WO reference clearly shows single MESI TLC state (e.g., I, S, E, M) and single MESI SLC state (e.g., I, S, E, M) transitioning to joint coherency state (e.g., SI, ES, EM, MI, II, MS, ...). The WO reference further shows a state diagram having the expanded states SI, ES, MI, MS, II, SS, EM, and MM, the first letter of a state line relating to the state in the TLC, while the second letter relates to the state in the SLC and/or in a lower cache hierarchy state; See Fig.3; page 12." Applicants respectfully but strongly disagree.

The Examiner is invited to read the brief description of figures on page 5 of the WO reference, where it states, "Figure 2 shows a state transition diagram of MESI states **according to the related art**, Figure 3 shows a state transition diagram of expanded MESI states **according to the present invention** ...." (emphases added). It is clear that what Figure 2 shows is a prior art which include only transitions from a single MESI state to another single MESI state. Only Figure 3 is related to what the invention is as disclosed in the WO reference. Please note that only expanded states are included in Figure 3 and there is no single MESI state in Figure 3 at all, as clearly stated by the brief figure description and by the detailed description of Figure 3 (page 12, par. 2, et seq.). The Examiner probably made the above quoted statements based on the table below the state transition diagram in Figure 3. That table shows what an expanded state really means. For example, if an "II" state means that a cache line in the CS (TLC) has an "I" state and its corresponding cache line in SLC has an "I" state.

It does not mean that there is actually a transition from a single MESI state to an expanded state at all. Figure 3 is specifically about transitions among expanded states used to optimize state transition diagram (see pages 12 and 13 of the WO reference) and it does not include any transition between a single MESI state and an expanded state. Thus, the WO reference does not teach or suggest the limitation of transitions from a single coherency state to a joint coherency state, as recited in the claims of the present application.

For the foregoing reasons, the combination of Arimilli_2 and the WO reference does not teach or suggest all of the limitations recited in independent claims 11, 14, 18, 21, 24, and 28. Thus, these claims are patentable over Arimilli_2 in view of the WO reference. Accordingly, all of the claims that depend therefrom are also patentable over Arimilli_2 in view of the WO reference. Applicant hereby respectfully requests that the Examiner withdraw the 35 USC § 103 rejections of claims 11-30.

CONCLUSION

Based on the foregoing, it is submitted that that all active claims are presently in condition for allowance, and their passage to issuance is respectfully solicited. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (503) 264-1700. Entry of this amendment is respectfully requested.

Respectfully submitted,

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